

CLAIMS

What is claimed is:

1 1. An apparatus comprising:  
2 a first component;  
3 a bus coupled to the first component, the bus to transmit packets of data; and  
4 a second component coupled to the bus, messages passed between the first  
5 component and the second component through packets transmitted on the bus.

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1 2. The apparatus of claim 1 wherein:  
2 the packets of data may include either data cycles or special cycles, the special  
3 cycles encoding messages.

1 3. The apparatus of claim 2 wherein:  
2 the second component may receive a message encoded in a special cycle from  
3 the first component and transfer that message to a third component, the third  
4 component coupled to the second component.

1 4. The apparatus of claim 3 wherein:  
2 the third component acts upon the message.

1           5. The apparatus of claim 3 wherein:  
2           the third component passes the message to a fourth component, the fourth  
3           component coupled to the third component.

1           6. The apparatus of claim 1 wherein:  
2           the second component receives a message from the first component and acts  
3           upon the message.

1           7. The apparatus of claim 6 wherein:  
2           the second component acts upon the message by asserting a signal.

1           8. The apparatus of claim 6 wherein:  
2           the second component acts upon the message by changing behavior of the  
3           second component.

1           9. A method of virtualizing signals comprising:  
2           receiving a signal in a first component;  
3           passing a first message from the first component through a bus, the message  
4           encoding information relevant to the signal; and  
5           receiving the first message in a second component through the bus.

1 10. The method of claim 9 wherein:  
2 the signal is a second message, the signal received by the first component from  
3 a third component.

1 11. The method of claim 9 wherein:  
2 the signal is a signal asserted by a third component.

1 12. The method of claim 9 further comprising:  
2 passing the first message from the second component through a second bus to a  
3 third component.

1 13. The method of claim 9 further comprising:  
2 acting on the first message, the acting performed by the second component in  
3 response to receiving the first message.

1 14. The method of claim 13 wherein:  
2 the acting comprises asserting a signal.

1 15. The method of claim 13 wherein:  
2 the acting comprises changing behavior.

1           16. A method of virtualizing signals in a system including a hub interface  
2 comprising:  
3           receiving a first signal in a first hub;  
4           passing a message from the first hub through a first hub interface, the message  
5 corresponding to the first signal; and  
6           receiving the message through the first hub interface in a second hub.

1           17. The method of claim 16 further comprising:  
2           acting on the message, the acting performed by the second hub responsive to  
3 the receiving the message.

1           18. The method of claim 17 wherein:  
2 the acting comprises asserting a second signal.

1           19. The method of claim 17 wherein:  
2 the acting comprises changing behavior.

1 20. The method of claim 16 further comprising:

2 determining if the message is intended for the second hub;

3 acting on the message if the determining indicates the message is intended for  
4 the second hub; and

5 passing the message through a second hub interface if the determining indicates  
6 the message is not intended for the second hub.

1 21. The method of claim 20 further comprising:

2 receiving the message in a third hub through the second hub interface.

1 22. A system using virtualized signals on a hub interface comprising:

2 means for receiving a first signal in a first hub;

3 means for passing a message from the first hub through a first hub interface, the  
4 message corresponding to the first signal, the first hub coupled to the first hub interface;  
5 and

6 means for receiving the message through the first hub interface in a second hub,  
7 the second hub coupled to the first hub interface.

1 23. The system of claim 22 further comprising:

2 means for acting on the message, the means for acting associated with the  
3 second hub and operating responsive to the means for receiving the message.

1 24. The system of claim 22 further comprising:

2 means for determining if the message is intended for the second hub;

3 means for acting on the message if the means for determining indicates the  
4 message is intended for the second hub;

5 means for passing the message through a second hub interface if the means for  
6 determining indicates the message is not intended for the second hub, the second hub  
7 interface coupled to the second hub; and

8 means for receiving the message in a third hub through the second hub interface,  
9 the third hub coupled to the second hub interface.

1 25. A chipset comprising:

2 a memory control hub capable of being coupled to a processor and capable of  
3 being coupled to a memory;

4 a bus coupled to the memory control hub, the bus implemented to transmit  
5 packets of data; and

6 an input-output hub coupled to the bus, the input-output hub capable of being  
7 coupled to an input-output device, the chipset capable of passing messages between  
8 the memory control hub and the input-output hub through packets transmitted on the  
9 bus, the messages including information about signals received from one or more of the  
10 processor, the memory, and the input-output device.

1        26. A system comprising:  
2        a processor;  
3        a processor bus coupled to the processor;  
4        a memory;  
5        a memory control hub coupled to the processor bus and coupled to the memory;  
6        a bus coupled to the memory control hub, the bus implemented to transmit  
7        packets of data;  
8        an input-output device; and  
9        an input-output hub coupled to the bus, the input-output hub coupled to the input-  
10       output device, wherein messages may be passed between the memory control hub and  
11       the input-output hub through packets transmitted on the bus, the messages including  
12       information about signals received from one or more of the processor, the memory, and  
13       the input-output device.

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